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10/640,349	08/12/2003	Yi-Fang Michael Shiuan	JCLA11051	7717

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 February 2008 and 04 April 2007</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-4,17 and 18</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-4,17 and 18</u> is/are rejected.

7)☒ Claim(s) <u>1 and 17</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>8/12/03 & 4/4/07</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

     1.☐ Certified copies of the priority documents have been received.

     2.☐ Certified copies of the priority documents have been received in Application No. _____.

     3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1.   Applicant's election of *Species I (i.e., claims 1-4, 17, and 18)* in the reply filed on 25 February 2008 is acknowledged and appreciated. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2.   Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

3.   The drawings were received on 4 April 2007. These drawings are acceptable (pertaining to adding "Prior Art" labels).

4.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: *"32," "33," "35," "36," "37," "39,"* and *"40"* (see Fig. 3); and *"40," "42," "43," "45,"* and *"50"* (see Fig. 4);. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the

specification to add the reference character(s) in the description in compliance with 37 CFR

1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any

amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. Each drawing sheet

submitted after the filing date of an application must be labeled in the top margin as either

"Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not

accepted by the examiner, the applicant will be notified and informed of any required corrective

action in the next Office action. The objection to the drawings will not be held in abeyance.

5.   The drawings have not been checked to the extent necessary to determine the presence of

all possible minor errors. Applicant's cooperation is requested in correcting any errors of which

applicant may become aware in the figures.

Specification

6.   The disclosure is objected to because of the following informalities:

        The term, "***techniques is introduced***" should be corrected, for example to, "***techniques***

are introduced" (see Page 5, Paragraph 9, Line 4).

        Appropriate correction is required.

7.   The specification has not been checked to the extent necessary to determine the presence

of all possible minor errors. Applicant's cooperation is requested in correcting any errors of

which applicant may become aware in the specification.

Claim Objections

8.   Claim 1 is objected to because of the following informalities:

The term, "***an non-responding period***" should be corrected, for example to, "***a non-***

responding period" (see Line 6).

Appropriate correction is required.

9.   Claim 17 is objected to because of the following informalities:

The term, "***an non-responding period***" should be corrected, for example to, "***a non-***

responding period" (see Line 7).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making
> and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it
> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
> contemplated by the inventor of carrying out his invention.

11.   Claims 17-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with

the written description requirement. The claims contains subject matter which was not described

in the specification in such a way as to reasonably convey to one skilled in the relevant art that

the inventors, at the time the application was filed, had possession of the claimed invention.

The claimed subject matter of "***self-adjusting CPU frequency***" (in line 6) is not described

in the specification. The present invention does not reasonably convey to one skilled in the

relevant art that the inventors, at the time the application was filed, had possession of a frequency

that adjusts itself.

12.   Claims 17-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with

the enablement requirement. The claims contains subject matter which was not described in the

specification in such a way as to enable one skilled in the art to which it pertains, or with which

it is most nearly connected, to make and/or use the invention.

        The claimed subject matter of **"self-adjusting CPU frequency"** (in line 6) is not described

in the specification. The present invention is not enabled for a frequency that adjusts itself.

13.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

14.   Claims 1-4, 17, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

15.   Claim 1 recites the limitation **"graphics data"** (in line 2). The lack of a grammatical

article (such as "a" or "a plurality of" or "the" or "said") preceding the limitation renders it

unclear whether the claim is establishing a new element; or instead referring back to some

preestablished limitation. For example, it would be unclear to an artisan whether a single element

of **"data"** is being claimed; or rather whether a plurality of **"data"** elements are being claimed.

16.   Claim 1 recites the limitation "*a system memory*" (in line 2). There is insufficient

antecedent basis for this limitation in the claim. It would be unclear to one having ordinary skill

in the art what, if any, "*system*" the memory is for. Is a "*system*" element a necessary component

of the invention?

17.   The abbreviation "*CPU*" in claim 1 (in line 3) is a relative term which renders the claim

indefinite. The abbreviation "*CPU*" is not defined by the claim, the specification does not

provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would

not be reasonably apprised of the scope of the invention. It would be unclear to one having

ordinary skill in the art what precisely "*CPU*" is intended to stand for. "Central processing unit"?

Or "critical patch update," for example?

18.   Claim 1 recites the limitation of "*power saving*" (in lines 5-6). There is insufficient

antecedent basis for this limitation in the claims. In particular, it would be unclear to one skilled

in the art what the comparative basis is for the aforementioned "*power saving*." The claim

provides no antecedent basis or guidance for any level or standard of power. For example: Is

there a power savings compared to some other undefined operating mode of the CPU? Or is

there a power savings compared to a conventional toaster oven (as one facetious example)?

19.   Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for

omitting essential structural cooperative relationships of elements, such omission amounting to a

gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "*a system memory*" (in line 2). It would be unclear to one having ordinary skill in the art what, if any, "*system*" the memory is for. Is a "*system*" element a necessary component of the invention?

An omitted structural cooperative relationship results from the claimed subject matter: "*a common clock source*" (in line 4). It would be unclear to one having ordinary skill in the art what claim element the clock source is "*common*" to. One or more of: The graphics display method? The graphics data? The multiple display devices? The computer? The system memory? And the CPU?

An omitted structural cooperative relationship results from the claimed subject matter: "*a power saving signal*" (in line 5) and "*a power saving process*" (in line 6). It would be unclear to one having ordinary skill in the art what the comparative basis is for the aforementioned "*power saving*." Does the signal/process save power simply by existing? Without a clear explanation of power level(s); an artisan has no reasonable way to determine when/how "power is saved."

An omitted structural cooperative relationship results from the claimed subject matter: "*a non-responding period*" (in line 6). It would be unclear to one having ordinary skill in the art what (if any) claim element is "*non-responding*" during such a period. Is the graphics display method non-responding? The graphics data? The multiple display devices? The computer? The system memory? The CPU? Furthermore, what claim element is not being responded to?

20.   Claim 1 recites the limitation "*the least common multiple occurrence of the blank periods*" (in line 7). There is insufficient antecedent basis for this limitation in the claim. There

is no earlier claimed subject matter of a "*multiple occurrence*" never mind a "*common multiple occurrence*".

21.   Claim 2 recites the limitation "*the executing step*" (in line 2). There is insufficient antecedent basis for this limitation in the claim. There isn't a single "*step*" recited in claim 1.

22.   Claim 3 recites the limitation "*the blank period*" (in line 1). There is insufficient antecedent basis for this limitation in the claim. Which one of the earlier claimed plurality of "*blank periods*" is intended to be the singular "*blank period*" here?

23.   Claim 17 recites the limitation "*graphics data*" (in line 2). The lack of a grammatical article (such as "a" or "a plurality of" or "the" or "said") preceding the limitation renders it unclear whether the claim is establishing a new element; or instead referring back to some preestablished limitation. For example, it would be unclear to an artisan whether a single element of "*data*" is being claimed; or rather whether a plurality of "*data*" elements are being claimed.

24.   Claim 17 recites the limitation "*a system memory*" (in line 2). There is insufficient antecedent basis for this limitation in the claim. It would be unclear to one having ordinary skill in the art what, if any, "*system*" the memory is for. Is a "*system*" element a necessary component of the invention?

25.   The abbreviation "**CPU**" in claim 17 (in line 3) is a relative term which renders the claim

indefinite. The abbreviation "**CPU**" is not defined by the claim, the specification does not

provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would

not be reasonably apprised of the scope of the invention. It would be unclear to one having

ordinary skill in the art what precisely "**CPU**" is intended to stand for. "Central processing unit"?

Or "critical patch update," for example?

26.   Claim 17 recites the limitation of "**power saving**" (in lines 5-6). There is insufficient

antecedent basis for this limitation in the claims. In particular, it would be unclear to one skilled

in the art what the comparative basis is for the aforementioned "**power saving**." The claim

provides no antecedent basis or guidance for any level or standard of power. For example: Is

there a power savings compared to some other undefined operating mode of the CPU? Or is

there a power savings compared to a conventional toaster oven (as one facetious example)?

27.   Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for

omitting essential structural cooperative relationships of elements, such omission amounting to a

gap between the necessary structural connections. See MPEP § 2172.01.

         An omitted structural cooperative relationship results from the claimed subject matter: "**a**

system memory" (in line 2). It would be unclear to one having ordinary skill in the art what, if

any, "**system**" the memory is for. Is a "**system**" element a necessary component of the invention?

         An omitted structural cooperative relationship results from the claimed subject matter: "**a**

common clock source" (in line 4). It would be unclear to one having ordinary skill in the art

what claim element the clock source is "***common***" to. One or more of: The graphics display

method? The graphics data? The multiple display devices? The computer? The system

memory? And the CPU?

An omitted structural cooperative relationship results from the claimed subject matter: "***a***

power saving signal" (in line 5) and "***a power saving process***" (in line 6). It would be unclear to

one having ordinary skill in the art what the comparative basis is for the aforementioned "***power***

saving." Does the signal/process save power simply by existing? Without a clear explanation of

power level(s); an artisan has no reasonable way to determine when/how "power is saved."

An omitted structural cooperative relationship results from the claimed subject matter:

"***self-adjusting CPU frequency***" (in line 6). It would be unclear to one having ordinary skill in

the art what (if any) claim element is "***self-adjusting***". Is the graphics display method doing the

adjusting? The graphics data? The multiple display devices? The computer? The system

memory? The CPU? Furthermore, what claim element is not being responded to? The present

invention is not enabled for a frequency that adjusts itself.

An omitted structural cooperative relationship results from the claimed subject matter: "***a***

non-responding period" (in line 7). It would be unclear to one having ordinary skill in the art

what (if any) claim element is "***non-responding***" during such a period. Is the graphics display

method non-responding? The graphics data? The multiple display devices? The computer? The

system memory? The CPU? Furthermore, what claim element is not being responded to?

28.   Claim 17 recites the limitation "***self-adjusting CPU frequency***" (in line 6). There is

insufficient antecedent basis for this limitation in the claim.

29.   Claim 17 recites the limitation "*the least common multiple occurrence of the blank*

periods" (in line 7). There is insufficient antecedent basis for this limitation in the claim. There

is no earlier claimed subject matter of a "*multiple occurrence*" never mind a "*common multiple*

occurrence".

30.   The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being

dependent upon rejected base claims.

Claim Rejections - 35 USC § 102

31.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on
> sale in this country, more than one year prior to the date of application for patent in the United States.

32.   Claims 1-4, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by

Shelton et al (US 6,046,709 A).

Claim Rejections - 35 USC § 103

33.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34.   This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c)

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

35.   Claims 1-4, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Shelton et al (US 6,046,709 A) in view of the **Applicants' Admitted Prior Art (AAPA)**.

Regarding claim 1, Shelton discloses a graphics display method for continuously

displaying graphics data on multiple display devices [Fig. 1; 113, 114, 116] of a computer [Fig.

1; 100, 102, 104] (see Column 6, Lines 11-27) that contains a system memory [e.g. frame buffer]

directly accessed by a CPU [Fig. 2; graphics boards 208, 210, 218, 220] (see Column 4, Lines

18-35), the method comprising:

using a common clock source [Fig. 4; 420] to synchronize blank periods of the display

devices (see Column 15, Lines 17-24);

receiving a power saving signal [Fig. 4; 404] from the CPU (see Column 15, Lines 8-16),

said power saving signal indicates a request for executing a power saving process [e.g. not

refreshing every display device as fast as possible] by the CPU during a non-responding period

(see Column 9, Lines 30-35 -- furthermore, Shelton's CPU isn't disclosed as "responding" to

voice commands, ambient brightness levels, or repugnant odors); and

executing the power saving process [i.e. frame locking] within the least common multiple

occurrence of the blank periods of the display devices [i.e., due to the slowest graphics board]

(see Column 4, Lines 47-64).

Shelton teaches, "*the master graphics board preferably also has **a reference clock*

*generator 420 that is **used to drive all reference clock lines for all synchronization cards and***

graphics boards** within the system. **This clock signal forms the basis for synchronizing video

***timing and buffer swaps**" (see Column 15, Lines 17-24).

Shelton continues, "**The vertical blank period should occur almost simultaneously for**

all monitors, __due to sync locking__, resulting in all displays 113, 114, 116 almost simultaneously

switching to the next frame in a corresponding set of frames. Such coordination is achieved by

__synchronizing the graphics boards 120 through an initialization process that sets all boards to__

__the same horizontal and vertical refresh frequencies__, and __directs the boards to follow a__

__common clock signal for timing initiation of the vertical refresh.__ This initialization is partially

controlled by the frame synchronization card" (see Column 7, Line 53 - Column 8, Line 5).

As such, Shelton clearly discloses using a common clock source to synchronize blank

periods of the display devices, as instantly claimed.

The instant application teaches that "**direct access**" can take place between a processor

and a memory unit "**through**" an intermediate circuit (see Page 4, Paragraph 7, Lines 9-11).

Therefore, the examiner finds no reasonable cause for an artisan to believe the instantly claimed invention is limited to a system memory directly connected to a CPU.

However, should it be shown that Shelton's graphics boards (208, 210, 218, 220) and frame buffer do not disclose a system memory [e.g. frame buffer] directly accessed by a CPU; the AAPA does disclose a graphics display method for continuously displaying graphics data on multiple display devices [Figs. 3 & 4; Display Devices] of a computer [Fig. 3; 30 & Fig. 4; 50] that contains a system memory [Figs. 3 & 4; System Memory] directly accessed by a CPU [Figs. 3 & 4; CPU] (see Page 5, Paragraph 8 - Page 6, Paragraph 10). The AAPA also discloses a system memory [Figs. 1 & 2; System Memory] directly accessed by a graphics board [Fig. 1 & 2; GFX] (see Page 4, Paragraph 7).

Shelton and the AAPA are analogous art, because they are from the shared inventive field of graphics display method for continuously displaying graphics data on multiple display devices. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the AAPA's "processor-to-system memory direct access control technique" with Shelton's "frame locking" power saving method, so as to limit the number of circuits that communication paths must traverse while synchronizing all the displays.

Regarding claim 2, Shelton discloses a step of detecting the upcoming least common multiple occurrence of the blank periods of the display devices before the executing step (see Column 10, Lines 20-43).

Regarding claim 3, Shelton discloses the blank period can be a horizontal blank period or a vertical blank period (see Column 3, Lines 10-25).

Regarding claim 4, Shelton discloses the horizontal blank period or the vertical blank period is provided by a graphics-processing unit [Fig. 2; 208, 210, 218, 220] (see Column 8, Lines 6-20).

Regarding claim 17, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Shelton discloses a graphics display method for continuously displaying graphics data on multiple display devices [Fig. 1; 113, 114, 116] of a computer [Fig. 1; 100, 102, 104] (see Column 6, Lines 11-27) that contains a system memory [e.g. frame buffer] directly accessed by a CPU [Fig. 2; graphics boards 208, 210, 218, 220] (see Column 4, Lines 18-35), the method comprising:

using a common clock source [Fig. 4; 420] to synchronize blank periods of the display devices (see Column 15, Lines 17-24);

receiving a power saving signal [Fig. 4; 404] from the CPU (see Column 15, Lines 8-16), said power saving signal indicates a request for executing a power saving process [e.g. not refreshing every display device as fast as possible] by self-adjusting CPU frequency (see Column 7, Line 53 - Column 8, Line 5) and a power level (see Column 11, Line 60 - Column 12, Line 6) during an non-responding period (see Column 9, Lines 30-35 -- furthermore, Shelton's CPU isn't disclosed as "responding" to voice commands, ambient brightness levels, or repugnant odors); and

executing the power saving process [i.e. frame locking] within the least common multiple

occurrence of the blank periods of the display devices [i.e., due to the slowest graphics board]

(see Column 4, Lines 47-64).

Shelton teaches, "*the master graphics board preferably also has __a reference clock__*

__generator 420 that is __used to drive all reference clock lines for all synchronization cards and__

__graphics boards__ within the system. __This clock signal forms the basis for synchronizing video__

__timing and buffer swaps__" (see Column 15, Lines 17-24).

Shelton continues, "***The vertical blank period should occur almost simultaneously for***

all monitors, __due to sync locking__, resulting in all displays 113, 114, 116 almost simultaneously

switching to the next frame in a corresponding set of frames. Such coordination is achieved by

__synchronizing the graphics boards 120 through an initialization process that sets all boards to__

__the same horizontal and vertical refresh frequencies__, and __directs the boards to follow a__

__common clock signal for timing initiation of the vertical refresh__. This initialization is partially

controlled by the frame synchronization card" (see Column 7, Line 53 - Column 8, Line 5).

As such, Shelton clearly discloses using a common clock source to synchronize blank

periods of the display devices, as instantly claimed.

The instant application teaches that "***direct access***" can take place between a processor

and a memory unit "***through***" an intermediate circuit (see Page 4, Paragraph 7, Lines 9-11).

Therefore, the examiner finds no reasonable cause for an artisan to believe the instantly claimed

invention is limited to a system memory directly connected to a CPU.

However, should it be shown that Shelton's graphics boards (208, 210, 218, 220) and frame buffer do not disclose a system memory [e.g. frame buffer] directly accessed by a CPU; the AAPA does disclose a graphics display method for continuously displaying graphics data on multiple display devices [Figs. 3 & 4; Display Devices] of a computer [Fig. 3; 30 & Fig. 4; 50] that contains a system memory [Figs. 3 & 4; System Memory] directly accessed by a CPU [Figs. 3 & 4; CPU] (see Page 5, Paragraph 8 - Page 6, Paragraph 10). The AAPA also discloses a system memory [Figs. 1 & 2; System Memory] directly accessed by a graphics board [Fig. 1 & 2; GFX] (see Page 4, Paragraph 7).

Shelton and the AAPA are analogous art, because they are from the shared inventive field of graphics display method for continuously displaying graphics data on multiple display devices. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the AAPA's "processor-to-system memory direct access control technique" with Shelton's "frame locking" power saving method, so as to limit the number of circuits that communication paths must traverse while synchronizing all the displays.

Regarding claim 18, Shelton discloses while executing the power saving process, the system memory is continuously accessed by the CPU during the non-responding period (see Column 6, Line 27 - Column 8, Line 5).

Response to Arguments

36.   Applicant's arguments filed 4 April 2007 have been fully considered but they are not persuasive.

The Applicants contend, "*First of all, Shelton et at. '709 fails to disclose, teach or suggest 'a system memory directly accessed by a CPU' as set forth in claims 1, 5, 8 and 12 (Emphasis added). It is asserted that the 'frame buffer', in Shelton, anticipated the 'system memory directly accessed by a CPU.' However, the system memory is the memory for entire computer system, which is connected to the CPU directly; while the Shelton disclosed the frame buffer, that is connected to the graphics chip, for storing the video data*" (see Page 11, Paragraph 3 of the reply filed 4 April 2007). However, the examiner respectfully disagrees.

The instant application teaches that "***direct access***" can take place between a processor and a memory unit "***through***" an intermediate circuit (see Page 4, Paragraph 7, Lines 9-11). Therefore, the examiner finds no reasonable cause for an artisan to believe the instantly claimed invention is limited to a system memory directly connected to a CPU.

As such, Shelton discloses a graphics display method for continuously displaying graphics data on multiple display devices [Fig. 1; 113, 114, 116] of a computer [Fig. 1; 100, 102, 104] (see Column 6, Lines 11-27) that contains a system memory [e.g. frame buffer] directly accessed by a CPU [Fig. 2; graphics boards 208, 210, 218, 220] (see Column 4, Lines 18-35).

However, should it be shown that Shelton's graphics boards (208, 210, 218, 220) and frame buffer do not disclose a system memory [e.g. frame buffer] directly accessed by a CPU; the AAPA does disclose a graphics display method for continuously displaying graphics data on multiple display devices [Figs. 3 & 4; Display Devices] of a computer [Fig. 3; 30 & Fig. 4; 50] that contains a system memory [Figs. 3 & 4; System Memory] directly accessed by a CPU [Figs. 3 & 4; CPU] (see Page 5, Paragraph 8 - Page 6, Paragraph 10). The AAPA also discloses a

system memory [Figs. 1 & 2; System Memory] directly accessed by a graphics board [Fig. 1 & 2; GFX] (see Page 4, Paragraph 7).

Shelton and the AAPA are analogous art, because they are from the shared inventive field of graphics display method for continuously displaying graphics data on multiple display devices. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the AAPA's "processor-to-system memory direct access control technique" with Shelton's "frame locking" power saving method, so as to limit the number of circuits that communication paths must traverse while synchronizing all the displays.

The Applicants contend, "*Secondly, Shelton et al. '709 does not disclose; teach or suggest 'a power saving process by the CPU during an non-responding period'. The Examiner alleges that 'Frame locking' of Shelton et al. '709 reads on the power saving process of the present invention as set forth in claims 1, 5, 8 and 12. During the power saving process, the CPU frequency and a power level are adjusted during the non-responding period for power saving, the invention can continuously display image/graphics data on a multiple display devices computer system when the CPU is executing the power saving process, as explained in the Para, [0034] of the specification of the invention*" (see Page 11, Paragraph 4 of the reply filed 4 April 2007). However, the examiner respectfully disagrees.

Shelton discloses receiving a power saving signal [Fig. 4; 404] from the CPU (see Column 15, Lines 8-16), said power saving signal indicates a request for executing a power saving process [e.g. not refreshing every display device as fast as possible] (see Column 4, Lines 47-64) by the CPU during a non-responding period (see Column 9, Lines 30-35 -- furthermore,

Shelton's CPU isn't disclosed as "responding" to voice commands, ambient brightness levels, or

repugnant odors).

The Applicants contend, "*However, Shelton et al. "709 teaches "[F]rame locking', as*

used herein, generally is the synchronization of the buffer swaps across multiple graphics boards

of corresponding frames'. Therefore, such a 'frame locking' is nothing to do with power saving

executed by the CPU as required for the present invention, as set forth in claims 1, 5, 8 and 12,

as currently amended and is distinct from the present invention as set forth in claims 1, 5, 8 and

12" (see Page 12, Paragraph 2 of the reply filed 4 April 2007). However, the examiner

respectfully disagrees.

Shelton explains, "*Synchronization by preferred embodiments the invention includes*

'frame locking' (described below). As used in this specification and claims that follow, a frame

represents a single image of a series of images that arc used to create a moving picture (also

referred to as a 'motion picture'). "Frame locking", as used herein, generally is the

synchronization of the buffer swaps across multiple graphics boards of corresponding frames.

Specifically, all buffer swaps take place for corresponding frames at approximately the same

time across multiple graphics boards. This causes the swap rate to be determined by the

graphics board that is rendering the most complicated image (i.e., the slowest graphics board),

so that no graphics board swaps faster than the slowest graphics board. In a preferred

embodiment, the frame synchronization cards are programmed so that the buffer swap takes

place during multiples of the vertical blank of each monitor. The vertical blank of each monitor

thus is synchronized to occur substantially simultaneously" (see Column 4, Lines 47-64).

Clearly, if Shelton's swap rate is lowered as determined by the slowest rendering graphics board, then there will be a power savings compared with the case of all the graphics boards swapping at their individual maximum rates.

The Applicants contend, "*Further, Shelton '709 fails to teach, disclose or suggest a step of 'using a common clock source to synchronize blank periods of the display devices' that is required for the present invention as set forth in claims 1 and 5. Shelton '709 teaches 'the master graphics board preferably also has a reference clock generator 420 that is used to drive all reference clock lines for all synchronization cards and graphics boards within the system' and '[T]his clock signal forms the basis for synchronizing video timing and buffer swaps' (Column 15, lines 17-24). However, Shelton herein does not specifically teach the reference clock generator 420 is used to synchronize any blank periods of the displays*" (see Page 12, Paragraph 3 of the reply filed 4 April 2007). However, the examiner respectfully disagrees.

Shelton teaches, "*the master graphics board preferably also has **a reference clock generator 420 that is used to drive all reference clock lines for all synchronization cards and graphics boards** within the system. **This clock signal forms the basis for synchronizing video timing and buffer swaps**"* (see Column 15, Lines 17-24).

Shelton continues, "***The vertical blank period should occur almost simultaneously for all monitors, due to sync locking, resulting in all displays 113, 114, 116 almost simultaneously switching to the next frame in a corresponding set of frames. Such coordination is achieved by synchronizing the graphics boards 120 through an initialization process that sets all boards to the same horizontal and vertical refresh frequencies, and directs the boards to follow a***

__common clock signal for timing initiation of the vertical refresh.__ This initialization is partially controlled by the frame synchronization card" (see Column 7, Line 53 - Column 8, Line 5).

As such, Shelton clearly discloses using a common clock source to synchronize blank periods of the display devices, as instantly claimed.

Applicant's arguments with respect to claims 1-4, 17, and 18 have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

37.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

        Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The

examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

        Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
15 May 2008